REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-30 are pending. Claims 1, 7-9, 11, 17-19, 21, 25, and 27-29 have been amended. Claims 6, 16, and 26 have been cancelled. No claims have been added. Therefore, claims 1-5, 7-15, 17-25, and 27-30 are now presented for examination.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-4, 6, 7, 10-14, 17, 20-22 and 24, 25 and 27 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,134,710 issued to Levine et al. (*Levine*). Applicant submits that claims1-4, 6, 7, 10-14, 17, 20-22 and 24, 25 and 27 are not anticipated by *Levine* for at least the reasons set forth below.

Claims 1-4, 6, 7, 10-14, 17 and 20

Claim 1 recites, in part, the following:

> **storing traces that are captured by the one or more hardware monitors** in a first level profile buffer, the first level profile buffer being architecturally non-visible memory;

Independent claim 11 recites similar limitations.

Levine is cited as teaching the limitations of claim 1. The cited portion of *Levine* states that the address of an instruction being executed is saved in a sampled instruction address register and the effective address of its operand is saved in a sampled data address register. See column 10, lines 63-67. Saving the address of an instruction is not equivalent to storing traces because the address of an instruction does not provide information about the actions performed by the instruction. Thus, Applicant submits that *Levine* does not teach or disclose storing traces that are captured by one or more hardware monitors, as recited in claim 1. Therefore, Applicant respectfully submits claims 1 and 11 are not anticipated by *Levine*.

Claims 2-4, 7 and 10 depend from claim 1. Claims 12-14, 17 and 20 depend from claim 2. Given that dependent claims necessarily include the limitations of the claims from which they depend, Applicant respectfully submits claims 2-4, 7, 10, 12-14, 17 and 20 are not anticipated by *Levine* for at least the reasons set forth above.

Claims 21, 22, 24, 25 and 27

Claim 21 recites, in part, the following:

> a first level profile buffer to initially store captured profiles, the first level profile buffer being architecturally non-visible;
> a second level profile buffer to receive captured profiles from the first level profile buffer, the second level profile buffer being architecturally visible

Thus, claim 21 recites a first level profile buffer to initially store captured profiles.

The cited portion of *Levine* states that the address of an instruction being executed is saved in a sampled instruction address register and the effective address of its operand is saved in a sampled data address register. See column 10, lines 63-67. Saving the address of an instruction is not equivalent to storing captured profiles because the address of an instruction does not provide any information about profiles of microarchitecture events. Thus, Applicant submits that *Levine* does not teach or disclose storing captured profiles in a first level profile buffer, as claimed by Applicant. Therefore, Applicant respectfully submits claim 21 is not anticipated by *Levine*.

Claims 22, 24, 25 and 27 depend from claim 21. Given that dependent claims necessarily include the limitations of the claims from which they depend, Applicant respectfully submits claims 22, 24, 25 and 27 are not anticipated by *Levine*.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 5, 15 and 23

Claims 5, 15 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Levine* as applied to claims 2, 12 and 22 respectively. Applicant submits that claims 5, 15 and 23 are not obvious in view of *Levine* for at least the reasons set forth below.

Claim 5, 15 and 23 depend from claims 1, 11 and 21, respectively. As discussed above, *Levine* fails to disclose at least one limitation of each of the independent claims. In particular, claims 1 and 11 recite storing traces that are captured by one or more hardware monitors and claim 21 recites a first level profile buffer to initially store captured profiles. These limitations are not taught or disclosed by *Levine*. Therefore, Applicant submits that claims 5, 15 and 23 are not obvious in view of *Levine*.

Claims 8, 9, 18, 19 and 28-30

Claims 8, 9, 18, 19 and 28-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Levine* in view of U.S. Patent No. 6,622,300 issued to Krishnaswamy et al. (*Krishnaswamy*). Applicant submits claims 8, 9, 18, 19 and 28-30 are not obvious in view of *Levine* and *Krishnaswamy* for at least the reasons set forth below.

Claims 8, 9, 18, 19 and 28-30 depend from independent claims 1, 11 and 21, respectively, and necessarily include the limitations of these independent claims. As discussed above, *Levine* fails to teach at least one limitation of each of the independent claims. *Krishnaswamy* is cited as disclosing receiving an interrupt or special event handler. Whether or not *Krishnaswamy* teaches the limitations as cited in the Final Office action, *Krishnaswamy* fails to cure the deficiencies of *Levine* in the independent claims, as discussed above. Therefore, Applicant respectfully submits claims 8, 9, 18, 19 and 28-30 are not obvious in view of *Levine* and *Krishnaswamy*.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-5, 7-15, 17-25, and 27-30 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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